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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,093	07/07/2003	Lars Erik Thon	AELU.P0006	8681
23349	7590	05/09/2005		EXAMINER
STATTLER JOHANSEN & ADELI				LAM, TUAN THIEU
P O BOX 51860				
PALO ALTO, CA 94303			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 05/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/615,093	THON, LARS ERIK <i>(CN)</i>
	<b>Examiner</b>	<b>Art Unit</b>
	Tuan T. Lam	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 11 April 2005.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 07 July 2003 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    - a) All    b) Some \* c) None of:
      1. Certified copies of the priority documents have been received.
      2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
      3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input checked="" type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                         | Paper No(s)/Mail Date. _____.   |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____.                                   |

## DETAILED ACTION

This is a response to the amendment filed 4/11/2005. Claims 1-20 are pending and are under examination.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7 and 11-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Shirani (US 2004/0193669).

Figure 1 shows a circuit comprising at least one delay element (LC circuits) for receiving a signal and for generating a time delay in said signal, calibration circuit (tuning circuit shown in figure 3), coupled to the delay element, for calibrating said delay element so as to match said time delay to a predetermined time period, and multiplier-summing circuit (18a-18n, 16a-16n and summing node) coupled to said delay element, for multiplying a signal output from said delay element and for summing said multiplied signal to generate and equalized signal as called for in claims 1 and 11.

Regarding claims 2, 4, 12 and 14, figure 3 shows the calibration circuit comprises a loop control (54, 56, 58) for receiving a reference signal (54), output from said delay element, and for generating a phase adjustment (output of the loop filter 58) based on said delay of said reference signal propagated through said delay element, and said delay element comprises selectable

parameters (varactor diodes) for receiving a phase adjustment from said control loop for setting said selectable parameters based on said phase adjustment.

Regarding claims 3 and 13, figure 3 shows a phase detector and a loop filter.

Regarding claims 5 and 15, the transmission lines are seen as the inductors.

Regarding claims 6 and 16, the capacitance of the varactor diodes are adjustable.

Regarding claims 7 and 17, inductor and varactor diodes are lumped elements.

3. Claims 1-5, 9-15 and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Roy et al. (US 2004/0131128).

Figure 4 shows a circuit comprising at least one delay element (delay elements 402, 404, 406) for receiving a signal and for generating a time delay in said signal, calibration circuit (tuning circuit shown in figure 5), coupled to the delay element, for calibrating said delay element so as to match said time delay to a predetermined time period, and multiplier-summing circuit (408, 410, 412, 414 and summing node) coupled to said delay element, for multiplying a signal output from said delay element and for summing said multiplied signal to generate and equalized signal as called for in claims 1 and 11.

Regarding claims 2, 4, 12 and 14, figure 5 shows the calibration circuit comprises a loop control (500) for receiving a reference signal (reference clock), output from said delay element, and for generating a phase adjustment (Vctl) based on said delay of said reference signal propagated through said delay element, and said delay element comprises selectable parameters for receiving a phase adjustment from said control loop for setting said selectable parameters based on said phase adjustment.

Regarding claims 3 and 13, figure 3 shows a phase detector inherently having a loop filter.

Regarding claims 5 and 15, the transmission lines are seen as wires.

Regarding claims 9 and 19, said delay element comprises a plurality of stub transmission lines (parallel paths).

Regarding claims 10 and 20, said delay element further comprises a means for selecting (switches 703, 705, 707, 709) a length of said stub transmission lines to calibrate said delay element (each parallel path has different transmission line length).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shirani (US 2004/0193669) in view of Yu et al. (US 2003/0090339).

Figure 1 of Shirani shows a circuit comprising at least one delay element (LC circuits) for receiving a signal and for generating a time delay in said signal, calibration circuit (tuning circuit shown in figure 3), coupled to the delay element, for calibrating said delay element so as to match said time delay to a predetermined time period, and multiplier-summing circuit (18a-18n, 16a-16n and summing node) coupled to said delay element, for multiplying a signal output from said delay element and for summing said multiplied signal to generate and equalized signal.

Shirani shows each delay element (inductor and varactor diode) is calibrated by a respective control signal (60a). Shirani does not show means for selecting combinations of said lumped parameters to calibrate said delay element as called for in claims 8 and 18. Figure 2 of Yu et al. shows a delay line having a plurality of delay elements, each delay element is calibrated by a selecting means (switches) to provide an accurate delay time and less sensitive to temperature fluctuation. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to replace each of Shirani's varactor diode with a switch and a capacitor for the purpose of providing an accurate delay time that is less sensitive to temperature fluctuation.

***Response to Arguments***

6. Applicant's arguments filed 4/11/2005 have been fully considered but they are not persuasive. Applicant argues that US patent application 2004/0193669 by Shirani filed Oct. 2, 2003 is not a prior art to the present invention filed July 7, 2003 is not persuasive. The applied US patent application 2004/0193669 has a provisional application 60/415,790, filed Oct. 2, 2002, discloses the subject matters, of figure 1 to figure 4c of the US patent application 2004/0193669, replied upon under the 35USC 102(e). Therefore, the subject matter disclosed therein has the priority date of Oct. 2, 2002 which is earlier than the effective filing date of the present invention. Therefore, the rejection of claims 1-7 and 11-17 is in compliance with the statutory section 102 (e). The rejection is remained.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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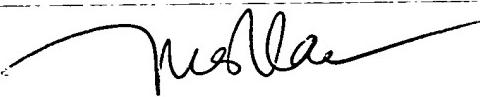
8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tuan T. Lam  
Primary Examiner  
Art Unit 2816